We claim:

SUB B1

1. A method of forming a semiconductor varactor, comprising:

forming a well region of a first conductivity type in a semiconductor substrate;

forming a gate dielectric layer on said well region;

forming a gate layer on said gate dielectric layer;

forming contact regions in said well region of a first conductivity type; and

forming gate layer contacts to said gate conductive layer wherein said gate layer contacts overlie said well region.

2. The method of claim 1 further comprising forming sidewall structures adjacent to said gate layer.

3. The method of claim 2 wherein said well region is n-type.

4. The method of claim 2 wherein said well region is p-type.

SUB B1

5. The method of claim 1 wherein said forming gate layer contacts comprises forming said gate layer contacts to said gate layer over an active area of said semiconductor varactor.

6. A semiconductor varactor, comprising:

a well region of a first conductivity type in a semiconductor substrate;

SUB B1

a gate dielectric layer on said well region;

a gate layer on said gate dielectric layer;

contact regions in said well region of a first conductivity type; and

gate layer contacts to said gate layer wherein said gate contacts overlie said well region.

7. The semiconductor varactor of claim 6 further comprising sidewall structures adjacent to said gate layer.

8. The semiconductor varactor of claim 7 wherein said well region is n-type.

9. The semiconductor varactor of claim 7 wherein said well region is p-type.

Sub B'

10. The semiconductor varactor of claim 6 wherein said gate layer contacts comprises gate layer contacts to said gate layer over an active region of said semiconductor varactor.

11. A method for forming a low resistance semiconductor varactor, comprising

providing a semiconductor substrate with at least a first isolation region and a second isolation region separated by a first distance;

SUB B1

forming a well region in said semiconductor substrate between said first isolation region and said second isolation region;

forming a contact isolation structure in said well region between said first isolation region and said second isolation region;

forming a gate dielectric layer on said well region and said contact isolation region;

forming a gate layer on said gate dielectric layer wherein said gate layer overlies said contact isolation region; and

forming electrical contacts to said gate conductive layer over said contact isolation region.

Sub B1

12. The method of claim 11 wherein said first and second isolation regions comprise STI structures.

13. The method of claim 11 wherein said contact isolation structure comprises a STI structure.

14. The method of claim 11 further comprising forming well contact regions adjacent to said first and second isolation regions.

15. A low resistance semiconductor varactor, comprising

providing a semiconductor substrate with at least a first isolation region and a second isolation region separated by a first distance;

SUB B1

a well region in said semiconductor substrate between said first isolation region and said second isolation region;

a contact isolation structure in said well region between said first isolation region and said second isolation region;

a gate dielectric layer on said well region and said contact isolation region;

a gate layer on said gate dielectric layer wherein said gate layer overlies said contact isolation region; and

electrical contacts to said gate conductive layer over said contact isolation region.

16. The varactor of claim 15 wherein said first and second isolation regions comprise STI structures.

17. The method of claim 15 wherein said contact isolation structure comprises a STI structure.

18. The method of claim 15 further comprising well contact regions adjacent to said first and second isolation regions.

19. A method of forming a semiconductor varactor, comprising:

forming a well region of a first conductivity type in a semiconductor substrate;

forming a gate dielectric layer on said well region;

forming a gate layer on said gate dielectric layer;

forming contact regions in said well region of a first conductivity type wherein said contact regions are formed using a source and drain region implantation formation process; and

forming gate layer contacts to said gate conductive layer wherein said gate layer contacts overlie an isolation region

20. The method of claim 19 further comprising forming sidewall structures adjacent to said gate layer.

21. The method of claim 20 wherein said well region is n-type.

22. The method of claim 20 wherein said well region is p-type.